

USB 2.0 High Speed 4-Port Hub Controller

Introduction

The FE1.1 is a highly integrated, high quality, high performance, low power consumption, yet low cost solution for USB 2.0 High Speed 4-Port Hub.

It adopts Multiple Transaction Translator (MTT) architecture to explore the maximum possible throughput. Six, instead of two, non-periodic transaction buffers are used to minimize potential traffic jamming. The whole design is based on state-machine-control to reduce the response delay time; no micro controller is used in this chip.

FE 1.1

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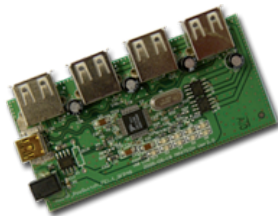
FE1.1 Order No. LQFP-48 (7x7mm Tray) or No. QFN-48 (6x6mm Tape&Reel)

To guarantee high quality, the whole chip is covered by Test Scan Chain – even on the high speed (480MHz) modules, so that all the logic components could be fully tested before shipping. Special Build-In-Self-Test mode is designed to exercise all high, full, and low speed Analog Front End (AFE) components on the packaging and testing stages as well.

Low power consumption is achieved by using 0.18µm technology and comprehensive power/clock control mechanism. Most part of the chip will not be clocked unless needed.

Evaluation-Board

available



Features

- Low power consumption
 - 115 mA when four downstream facing ports enabled in High-Speed mode
 - 64 mA when one downstream facing port enabled in High-Speed mode
- Fully compliant with Universal Serial Bus Specification Revision 2.0 (USB 2.0)
 - Upstream facing port supports High-Speed (480MHz) and Full-Speed (12MHz) modes mode
 - 4 downstream facing ports support High-Speed (480MHz), Full-Speed (12MHz), and Low-Speed (1.5MHz) modesh-Speed mode
- Integrated USB 2.0 Transceivers
- Integrated upstream 1.5KΩ pull-up, downstream 15KΩ pull-down, and serial resistors
- Integrated 5V to 3.3V and 1.8V regulator
- Integrated Power-On-Reset circuit
- Integrated 12MHz Oscillator with feedback resistor, and crystal load capacitance
- Integrated 12MHz-to-480MHz Phase LockLoop (PLL)
- Multiple Transaction Translators (MTT)
 - One TT for each downstream port
 - Alternate Interface 0 for Single-TT, and Alternate Interface 1 for Multiple-TT
 - Each TT could handle 64 periodic Start-Split transactions, 32 periodic Complete-Split transactions, and 6 non-periodic transactions
- Automatic self-power status monitoring
 - Automatic re-enumeration when Self-Powered switching to Bus-Powered
- Board configured options:
 - Ganged or Individual Power Control Mode select
 - Global or Individual Over-Current
 - Detection Mode select
 - Removable or Non-Removable Downstream Devices configuration
- Comprehensive status indicators support:
 - Standard downstream port status indicators (Green and Amber LED control for each downstream port)
 - Hub active LED support



-40°C - 85°C

Order Information FE1.1 LQFP-48*) extended temperature range

*) Product of order code LQFP-48 is finally tested in Room Temperature, 85° and -40°C, respectively.