FE12.3

USB 2.0 High Speed 4-Port Hub Controller

Product Brief

Introduction

Based on world renown and well time-tested FE1.1s design, the FE12.3 provided one extra feature: Bypass mode. Setting it to BYPASS Mode will make upstream port to downstream port 1 conduct as a direct line. Its purpose is to allow OTG connection between SOC USB HOST and external device through FE12.3.

As the FE1.1s, The FE12.3 is a highly integrated, high quality, high performance, low power consumption, yet low cost solution for USB 2.0 High Speed 4-Port Hub. With its tiny footprint, it is the best choice for embedded application.

It adopts *Multiple Transaction Translator* (MTT) architecture to explore the maximum possible throughput. Six, instead of two, non-periodic transaction buffers are used to minimize potential traffic jamming. The whole design is based on state-machine-control to reduce the response delay time; no micro controller is used in this chip.

To guarantee high quality, the whole chip is covered by *Test Scan Chain* – even on the high speed (480MHz) modules, so that all the logic components could be fully tested before shipping. Special Build-In-Self-Test mode is designed to exercise all high, full, and low speed Analog Front End (AFE) components on the packaging and testing stages as well.

Low power consumption is achieved by using LPM (*Link Power Management*) feature and comprehensive power/clock control mechanism. Most part of the chip will not be clocked unless needed.

The FE12.3 could be optionally configured to support Charging Downstream Ports as defined by USB-IF *Battery Charging Specification*. With this feature enabled, an USB hub could be easily transformed into a charging station – *USB Charging Hub* for *Universal Charging Solution* compliant battery based portable devices.

Features

- Fully compliant with Universal Serial Bus Specification Revision 2.0 (USB 2.0);
  - Upstream facing port supports High- Speed (480MHz) and Full-Speed (12MHz) modes;
  - 4 downstream facing ports support High-Speed (480MHz), Full-Speed (12MHz), and Low-Speed (1.5MHz) modes;
- Compliant with Universal Charging

Solution, and USB Battery Charging Specification 1.1/1.2;

- USB Link Power Management (LPM) support;
- Integrated USB 2.0 Transceivers;
- Integrated upstream 1.5KΩ pull-up, downstream 15KΩ pull-down, and serial resisters;
- Integrated 3.3V to 1.8V regulator.
- Integrated Power-On-Reset circuit;
- Integrated 12MHz Oscillator with feedback resister, and crystal load capacitance;
- Integrated 12MHz-to-480MHz Phase Lock Loop (PLL);
- Integrated Portable Device detection circuitry for UCS supporting;
- Multiple Transaction Translators (MTT) –
  - One TT for each downstream port;
  - Alternate Interface 0 for Single-TT, and Alternate Interface 1 for Multiple-TT;
  - Each TT could handle 64 periodic Start-Split transactions, 32 periodic Complete-Split transactions, and 6 none-periodic transactions;
- Automatic self-power status monitoring;
  - Automatic re-enumeration when Self-Powered switching to Bus-Powered;
- Board configured options –
  - Support of portable device detection mechanism for Universal Charging Solution on downstream ports;
  - ***BYPASS Mode*** select;

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